CLAIMS:

1. In a memory device having plural DRAM sub-arrays, each with plural array rows, the improvement comprising:

an address decoder for decoding an address of a memory access request and indicating which of the plural DRAM sub-arrays are referenced by the memory access request; and

refresh circuitry, responsive to the indication of the address decoder, to refresh at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request while substantially contemporaneously performing the memory access request.

2. The memory device as claimed in claim 1, wherein the memory access request comprises a read access request.

3. The memory device as claimed in claim 2, further comprising a non-array row, external to the plural DRAM sub-arrays, for receiving from the DRAM sub-array referenced by the address of the read access request at least a portion of an array row corresponding to the address of the read access request.

4. The memory device as claimed in claim 3, wherein the non-array row comprises an SRAM row.

5. The memory device as claimed in claim 3, further comprising:

a tag register for storing at least a portion of the address of a read access request that last stored information into the non-array row; and

a command decoder for signaling that the read access request may be serviced from the non-array row rather than the array row corresponding to the address of the read access request.

6. The memory device as claimed in claim 1, wherein the memory access request comprises a write access request.

7. The memory device as claimed in claim 6, further comprising a non-array row, external to the plural DRAM sub-arrays, for storing, prior to

writing to the DRAM sub-array referenced by the address of the write access request, at least a portion of an array row corresponding to the address of the write access request.

8. The memory device as claimed in claim 1, wherein the refresh circuitry further comprises a refresh timer for limiting a frequency of refreshes performed.

9. The memory device as claimed in claim 8, wherein the refresh circuitry further comprises a missed refresh counter for tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays.

10. The memory device as claimed in claim 1, wherein the refresh circuitry further comprises a refresh counter for storing a next array row to be refreshed in at least one of the plural DRAM sub-arrays.

11. A method of refreshing a memory device having plural DRAM sub-arrays, each with plural array rows, the method comprising:

(a) decoding an address of a memory access request;

(b) indicating which of the plural DRAM sub-arrays are referenced by the memory access request;

(c) refreshing, in response to the indicating step, at least one array row of at least one of the plural DRAM sub-arrays not referenced by the memory access request; and

(d) executing the memory access request,

wherein steps (c) and (d) are performed substantially contemporaneously.

12. The method as claimed in claim 11, wherein the memory access request comprises a read access request.

13. The method as claimed in claim 11, further comprising:

receiving, into a non-array row external to the plural DRAM sub-arrays and from the DRAM sub-array referenced by the address of the read access request, at least a portion of an array row corresponding to the address of the read access request.

14. The method as claimed in claim 13, wherein the step of receiving comprises receiving the portion into an SRAM row.

15. The method as claimed in claim 14, further comprising:

storing in a tag register at least a portion of the address of a read access request that last stored information into the non-array row; and

comparing whether the read access request may be serviced from the non-array row rather than the array row corresponding to the address of the read access request.

16. The method as claimed in claim 11, wherein the memory access request comprises a write access request.

17. The method as claimed in claim 16, further comprising storing into a non-array row, external to the plural DRAM sub-arrays, prior to writing to the DRAM sub-array referenced by the address of the write access request, at least a portion of an array row corresponding to the address of the write access request.

18. The method as claimed in claim 11, further comprising limiting a frequency of refreshes performed based on a refresh timer.

19. The method as claimed in claim 18, further comprising tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays.

20. The method as claimed in claim 11, further comprising updating a refresh counter to store a next array row to be refreshed in at least one of the plural DRAM sub-arrays.

21. In a memory device having a non-array row external to plural DRAM sub-arrays, for receiving from the DRAM sub-array referenced by an address of an access request, the improvement comprising:

a command decoder for internally determining when a refresh cycle can be hidden behind an access to the non-array row; and

a controller for limiting refresh cycles to a subset of possible times internally determined by the command decoder.

22. The memory device as claimed in claim 21, wherein the non-array row comprises an SRAM row.

23. The memory device as claimed in claim 21, wherein the controller comprises a missed refresh counter for tracking a number of refreshes missed by at least one of the plural DRAM sub-arrays.

24. The memory device as claimed in claim 21, wherein the controller further comprises a refresh counter for storing a next array row to be refreshed in at least one of the plural DRAM sub-arrays.